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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,350	GREENBERG, STEVEN S.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2000*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 have been presented for reconsideration in view of Applicant's arguments.

Response to Arguments

2. Applicant's arguments submitted in the 15 June 2004 response have been fully considered. The Examiner's response is as follows.

2.1 Regarding the Applicant's response to the use of the *Steinman Patent U.S. Patent 5,794,005* as non-analogous art.

Applicant argued:

> Claim 1's method is to be used in a single computer. Applicant submits that the Steinman Patent is not within the just-described field of invention. This is because the Steinman patent is in the field of discrete event simulation of objects using a plurality of synchronous parallel computers in communication with each other so that objects being simulated may interact (emphasis added; see Steinman's "Technical Field" description at column 1, lines 26-30). A reference from parallel computing is not within the field of performing mixed-signal simulation in a single computer.

The Examiner has reviewed Applicant's specification and finds no support for the argument that *"parallel processing"* during a simulation, teaches away from Applicant's preferred embodiment. The Examiner notes that parallel computing can be performed on a single computer by using a multiple processors and that nowhere in Applicant's claim language is there described, a digital computer, *with only one processor.* Further, the Examiner while performing an updated search found another patent issued to the same inventor and which incorporates the *Steinman* reference. In the new *Steinman* reference, U.S. Patent 5,850,538, *hereafter referred to as the Steanman538 reference,* is disclosed in **Col. 2 Lines 56-58,** the following, *"the Qheap and the event horizon applied to the priority queues is applicable in aiding* ***both*** *paralell and*

sequential discrete-event simulation." Thus the *Steinman538* reference clearly teaches that there is a difference between parallel and discrete-event simulation and further, there is no teaching in the *Steinman538* reference that precludes the use of a single digital computer. Further, the *Steinman538* reference teaches in **Col. 6 Lines 54-57,** *"However, it should be noted that the Qheap is a new priority queue in itself and can be used with* ***numerous*** *computer applications requiring a priority queue."* Thus, the *Steinman538* reference discloses that in no way are the simulation methods disclosed restricted from being used on a single computer. Therefore *Steinman* reference is analogous art.

Applicant argued:

Specifically, the undersigned has carefully reviewed Figures 1-16 of the Steinman Patent and found no disclosure whatsoever of "a simulation model for digital circuits".

It is noted by the Examiner that the *Steinman* reference was relied upon *only* for teaching a generic modeling method used in any type of simulation, *including the simulation of digital circuits* and that the *Buch et al.* reference was relied upon to teach the specific simulation of digital/analog mixed signal simulations.

2.2 Regarding the Applicants response to the use of the *Buch* reference.

Applicant argued:

"the **Buch reference states** that **some simulation frameworks** that interface fast, event-driven digital simulations with time point-driven analog simulators **can have problems** handling strong feedback from analog to digital (and vice versa) subcircuits (see bottom of left column on page 403)."

And...

The Examiner is hereby requested to explicitly state in the next Office Action their basis for a **reasonable expectation of success** in overcoming such documented problems.

As requested by the Applicant, the Examiner will now show how the *Buch* reference itself provides the basis for success in overcoming the challenges of simulating a mixed analog and digital circuit. On page 403 of the *Bush* in the right column is disclosed the following:

*"Dynamic circuit partitioning is combined with an event-driven approach to exploit the latency and multi-rate behavior, and efficiently handle tight coupling and **feedback** in the circuit." (page 403, right column, SYMPHONY: A Fast Mixed Signal Simulator for BiMOS Analog/Digital Circuits" by Premal Buch and Ernest S. Kuh.)*

To clearly answer the Applicant's question, Dynamic circuit partitioning, which is provided by using object oriented methods, as disclosed in the *Steinman* reference **(Figure 1 Item 1,** and specifically the flow chart in **Figure 15,** note the section of the algorithm where the state of the simulation object is changed, this state change could be the result of a feedback signal being simulated, because the rest of the simulation has continued, there is a requirement to *"rollback"* the simulation to a point before the feedback was taken into account and now add in the result of the feedback, as disclosed in **Figure 16,** once this action has occurred, then the event can be *"reprocessed"* as disclosed in item **178** and the simulation continues.**)** The *lazy cancellation* approach, **(Steinman Col. 5 Lines 5-15),** and specifically the *"breathing time buckets"* as disclosed in **Figure 3** provide a flexible and efficient method of managing events during the execution of a simulation even if the inputs values, *provided from feedback,* would produce a different result.

2.3 Regarding the Applicant's response to the rejection of Claim 1 using the *Steinman* reference where the reference teaches the use of a hash function and a heap.

Applicant argued;

> While the Steinman Patent Appears to disclose hash buckets, there is no indication whatsoever that the hash buckets are to be used with priority heaps.

The Examiner notes that limitations of hash buckets and heaps are disclosed as, *known in the art,* methods of managing events in simulations by the *Steinman* reference. The Applicant's claims are directed towards using hash values for the event times in the hash buckets and then organizing the times into heap. The heap data structure is well known in the computer art, specifically, a heap is defined as, A portion of memory reserved for a program to use for the temporary storage of data structures whose existence or size cannot be determined until the program is running," *Microsoft Press Computer Dictionary Third Edition pages 229 and 230.*

2.3 Regarding Applicant's response to the use of the *Ulrich* reference in the 35 U.S.C. 103 rejections of Claims 1-18.

Applicant argued;

> Applicant respectfully submits that although the Ulrich reference mentions non-integral event timing in its title, the method disclosed in the "The Event Scheduling Process" (right column on page 61 and the bottom half of page 62) subdivides the time axis between two integral times into a "large" number of intervals (the example in Fig. 2 uses 8, the text later states 256 or 512). The implication of these numbers of intervals is that the Ulrich reference uses an integral time with a higher resolution than a time unit (1/8 for the example, 1/256 or 1/512 for the text).

The Examiner notes that none of the definitions or descriptions presented as arguments as to why the *non-integral* methods presented in the *Ulrich* reference teach away from the

Applicant's current claim language are present in the current claim language. Although Applicant's arguments may be correct in relationship to the instant specification, because of the lack of a specific definition, as disclosed in the specification, and pointed to by the Applicant, combined with the lack of *"means for"* or *"means plus function"* language in the claims, the Examiner has demonstrated that a reasonably broad interpretation of the claim language, in regards to the term *non-integral,* is anticipated by the *Ulrich* reference. Further, it is noted by the Examiner that the *Ulrich* reference is directed towards simulation of digital circuits.

Applicant argued:

In a future Office Action, the Examiner is hereby requested to provide a **pin-point citation** of a single line or a handful of lines where in Ulrich teaches an efficiency advantage that the Examiner cites.

The Examiner notes the following discussion as disclosed on page 61, right hand column, of the *Ulrich* reference;

"Combining a time-mapping table (time-wheel) with multiple linear list permits the breaking up of a long linear list (Fig. 1) into short individual lists (Fig. 2) for which event scheduling can be done more ***efficiently.****"*

The Examiner has found Applicant's arguments to be unpersuasive and upholds the 35 U.S.C. 103(a) rejections of **Claims 1-18**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005** in view of **Steinman U.S. Patent 5,850,538** *hereafter referred to as the Steinman538 reference* and in further view of **"SYMPHONY: A Fast Mixed Signal Simulator for BiMOS Analog/Digital Circuits"** by Premel Buch and Ernest S. Kuh hereafter referred to as the *Buch et al.* reference and in further view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich* reference.

3.1 As regards independent **Claim 1** the *Steinman* reference discloses scheduling events in a simulation model, *which could be used for modeling digital circuits,* **(Figures 1-16 specifically Figure 1 Items 15 and 16 describe a "Generic Object Event Queue"** and that Generic Object could be a *Digital Circuit being simulated* and **Figure 15** checks the state of the simulation object, **item 156),** using hash buckets **(Figures 4 and 5),** organizing the scheduled times into a *priority* heap **(Col. 8 Lines 53-58),** associating scheduled times assigned to the events in the buckets **(Figure 3, 4, 5, 6, 7, 8, 9, Col. 8 Lines 27-67, Col. 9 Lines 1-51),**

removing a earliest scheduled time from the heap **(Figure 14 Items 132, 136 and 110, Col. 10 Lines 49-53),** re-organizing the remaining scheduled times into a new configuration **(Col. 14 Lines 34-54),** and repeating the steps until the queue is empty **(Figure 15 Items 150, 152, 154 and 156).** Further, the *Steinman538* reference discloses that the methods disclosed in both *Steinman* refenreces can be used for both parallel and sequential discrete-event simulation ***(Steinman538 Col. 2 Lines 56-58),*** and that these methods can be used for many types of simulations ***(Steinman538 Col. 2 Lines 35-41)*** and that the priority queue methods disclosed can be used with numerous computer applications requiring a priority queue ***(Steinman538 Col. 6 Lines 54-57)*** and it is noted that the *Steinman* **5,794,005** reference is incorporated into the *Steinman538* reference and therefore the two references are combined. It is further noted that the *Steinman538* reference discloses tree figures **(Figures 5, 6, 7 and 8),** that are identical in structure to the figures disclosed in Figures **2A and 2B** of Applicant's specification.

However the *Steinman* reference does not expressly disclose events occurring at non-integral times and mixed signaling for mixed analog and digital circuits in a simulation model.

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of ordinary skill in the art, presented with the problem of simulating a mixed signal integrated circuit would have been motivated to find a method of handling the scheduling of events in a mixed signal circuit simulation. In the related art of mixed signal simulation the *Buch et al.* reference discloses a method of handling event synchronization in a mixed analog and digital circuit simulation **(Page 404 section 2.2 Event Management).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the analog-digital mixed signal simulation event handling technologies of the *Buch et al.* reference because the *Symphony* technology provides a mixed signal simulator for designs with bipolar devices that is efficient **(Buch et al. page 407 Conclusions).**

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of ordinary skill in the art, presented with the problem of simulating digital logic would want to have an algorithm that is more efficient. In the same art of digital simulation, the *Ulrich* reference discloses a more efficient method of simulating digital circuits **(pages 61-67).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the non-integral event timing technologies of the *Ulrich* reference because, the *Ulrich* reference teaches a method of reducing un-needed delays as well as removing the possibility of having zero-delay race conditions during the simulation **(page 67).**

3.2 As regards dependent **Claim 2** the *Steinman* reference does not expressly disclose a method of determining events in a mixed signal simulation of digital and analog circuits.

In the related art of analog/digital circuit simulation, the *Buch et al.* reference discloses a method of determining events in a mixed signal simulation **(page 404 Event Management).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the *hash bucket* simulation technologies of the *Steinman*

reference with the *event management* technologies of the *Buch et al.* reference because of the improved performance of mixed signal simulations provided by the methods in the *Buch et al.* reference **(page 407).**

3.3 As regards dependent **Claims 3 and 4** the *Steinman* reference teaches the handling of new events **(Figure 13 Item 58).**

4. **Claims 5-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005** in view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich* reference.

4.1 Regarding independent **Claims 5, 11 and 16** the *Steinman* reference discloses scheduling events for associated scheduled times **(Figures 2 and 11),** and storing the events into buckets **(Figure 3),** and organizing the scheduled times into a structure, wherein the structure is constructed and arraigned to allow easy location of an earliest scheduled time **(Figure 2).**

However, the *Steinman* reference does not expressly disclose non-integral time events.

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of ordinary skill in the art, presented with the problem of simulating digital logic would want to have an algorithm that is more efficient. In the same art of digital simulation, the *Ulrich* reference discloses a more efficient method of simulating digital circuits **(pages 61-67).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman*

reference with the non-integral event timing technologies of the *Ulrich* reference because, the *Ulrich* reference teaches a method of reducing un-needed delays as well as removing the possibility of having zero-delay race conditions during the simulation **(page 67).**

4.1 As regards dependent **Claim 6** the *Steinman* reference discloses a hash table **(Figures 4 & 5).**

4.2 As regards dependent **Claim 7** the *Steinman* reference discloses a specific scheduled time for events **(Figures 8 & 9).**

4.3 As regards dependent **Claims 8 & 9** the *Steinman* reference discloses a heap **(Col. 8 Lines 53-58).**

4.4 As regards dependent **Claim 10** the *Steinman* reference discloses events, buckets and scheduled times **(Figures 2 & 3).**

4.5 As regards dependent **Claims 11-13** the *Steinman* reference discloses checking to see if the event is done **(Figure 15 Item 152)** and managing event queues **(Figure 1-16).**

4.6 As regards dependent **Claim 15** the *Steinman* reference discloses hash tables **(Figure 3 & 4).**

4.7 As regards dependent **Claim 17** the *Steinman* reference discloses heaps **(Col. 8 Lines 53-58).**

5. Dependent **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005 Steinman U.S. Patent 5,850,538** *hereafter referred to as the Steinman538 reference* and in further view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich*

reference and in further view of **"SYMPHONY: A Fast Mixed Signal Simulator for BiMOS Analog/Digital Circuits"** by Premel Buch and Ernest S. Kuh hereafter referred to as the *Buch et al.* reference.

5.1 As regards independent **Claim 16** see paragraph **4.1** above.

5.2 As regards dependent **Claim 17** the *Steinman* reference does not expressly disclose mixed signal simulation.

The *Buch et al.* reference discloses mixed signal simulation **(Page 404 section 2.2 Event Management).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the analog-digital mixed signal simulation event handling technologies of the *Buch et al.* reference because the *Symphony* technology provides a mixed signal simulator for designs with bipolar devices that is efficient **(Buch et al. page 407 Conclusions).**

Conclusion

6. **Claims 1-18** have been presented for reconsideration in view of Applicant's arguments. **Claims 1-18** have been reconsidered and rejected. The arguments presented by the Applicant in regards to the suitability of the *Steinman* reference as teaching the use of a single computer and further the suitability of the disclosed event management methods for use in a sequential discrete-event simulation have required that the Examiner to clarify the suitability of the earlier rejections by adding the second *Steinman* reference, U.S. Patent 5,850,538. The expanded 35

U.S.C. 103 rejections of Claims 1-18 were required to respond properly to Applicant's arguments.

6.1 Applicant's arguments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER